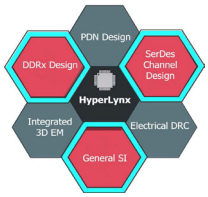
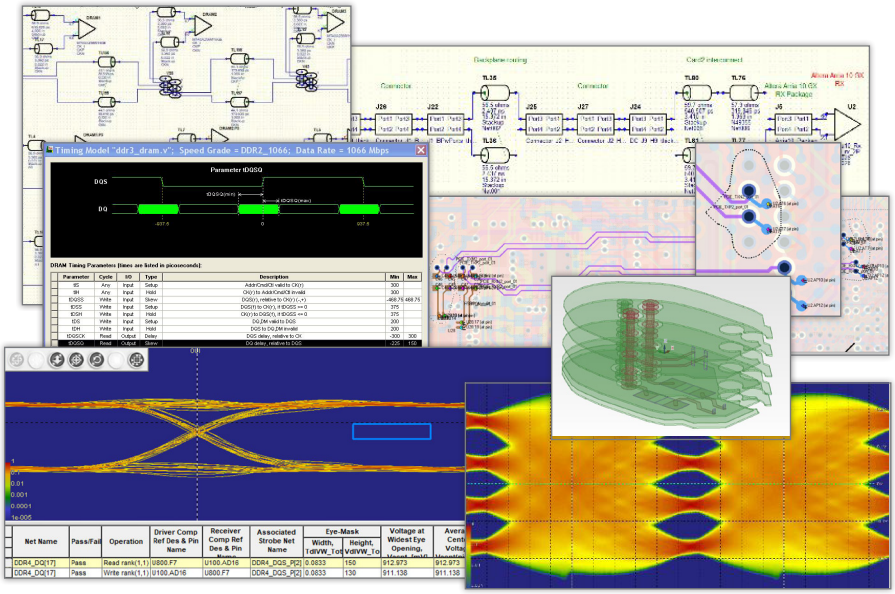


HyperLynx SI

DDR, SerDes, General Purpose Signal Integrity

DATASHEET



HyperLynx SI supports pre- and post-layout signal integrity, timing, crosstalk, and power-aware simulation. Automated workflows support complete interface-level DDRx verification and compliance analysis of standards-based SerDes channel designs.

Overview

Signal integrity simulation is often seen as a task best left to dedicated specialists, but there are not enough specialists to meet today's demand. HyperLynx SI combines industry-renowned ease of use with automated workflows to make complex SI analysis tasks accessible to system design engineers while still providing the detailed modeling and simulation accuracy demanded by signal integrity experts.

HyperLynx post-route (BoardSim) simulations automatically extract models of the PCB design as-routed, determining high-speed signal voltage and timing margins. Potential issues can be identified and resolved before the PCB is fabricated, reducing costs and delays associated with prototype spins. Pre-route simulations are key during PCB floor planning and routing, performing "what-if" analysis to determine the impacts of different design strategies. The HyperLynx topology editor (LineSim) allows quick capture of complex topologies and can sweep design variables to establish which physical design approach is best. HyperLynx automated workflows walk users through setting up and running complex analyses step by step, producing HTML reports with detailed margin measurements and associated plots.

KEY FEATURES

- Industry-renowned ease of use makes advanced SI simulation accessible to design engineers
- Sophisticated modeling and simulation techniques meet the needs of SI specialists
- Complete workflows for DDRx and SerDes channel analysis
- Pre-route topology editor with crosstalk and swept-parameter supports quick "what-if" decisions during design
- Automated post-route PCB extraction and simulation provides rapid PCB verification before release to manufacturing
- Interactive and batch mode simulation support
- Automatically identifies critical high-speed areas and solves with integrated 3D EM solver
- Supports multiple simulation engines for different component modeling strategies
- Seamlessly integrates with HyperLynx PI to provide full system level analysis
- Works with all major PCB layout systems

Advanced DDRX And SerDes Channel Support

HyperLynx SI provides complete automated workflows for DDRx interface and compliance-based SerDes channel design. The same workflows support both pre- and post-route analysis, letting designers perform both pre-route tradeoff analysis and post-route verification with the same simulation flow. The DDRx Wizard performs signal integrity and timing analysis across an entire DDRx interface, analyzing all signals and their relationships for compliance with both JEDEC standards and controller specifications. The DDRx flow includes an optional power-aware analysis capability that analyzes the impact of driver SSO/SSN and non-ideal signal return paths on system design margins.

The SerDes Compliance Wizard provides a common analysis flow across a wide selection of popular standard protocols, automatically adapting the type of analysis performed and reported metrics based on the selected protocol. The SerDes Compliance Wizard supports frequency-domain mask, time-domain mask, Channel Operating Margin (COM) and JCOM-based analysis.

Pre-Route Design Planning

Pre-route SI identifies signal integrity issues early to drive PCB placement and routing. Evaluate different stackups, optimize signal topologies, terminations, via designs and spacing values. The LineSim graphical editor helps you get it right the first time.

- Drag and drop editing of ICs, traces, vias, cables, connectors and passive components lets you capture and simulate complex designs on the fly
- Crosstalk analysis trades off spacing against design margins
- Integrated 2D and 3D EM solvers provide highly accurate models of traces, vias and other structural elements
- Easily instantiate IBIS, S-parameter, IBIS-AMI, HSPICE, ELDO, and AMS device models
- Interactive simulation lets you immediately see impact of design changes on signal quality, crosstalk, etc.
- Swept-parameter analysis quantifies effects of design variables on circuit behavior

Post-Route Verification

Post-route SI is used to sign-off a completed PCB before manufacture, reducing the risk of prototype spins. HyperLynx SI can analyze a board all through the layout process - after part placement, during critical net routing and after the board is complete. This lets designers find and resolve SI issues as soon as possible.

- Batch mode simulation provides fast scanning of an entire design for basic issues
- DDRx and SerDes Compliance wizards automate detailed analysis of entire interfaces to determine design margins
- Interactive simulation allows real-time investigation of problem areas with “what-if” analysis
- Automatic post-route topology extraction, including return path aware 3D modeling
- Powerful, easy-to-use multi-board analysis, including support for EBD and connector models
- User-defined crosstalk thresholds make it easy to browse the layout and visually identify coupling issues
- Ability to turn different physical effects on/off: quantifies the effect of different phenomena on design margins
- Interface to full-wave 3D field solver allows for extraction and analysis of complex layout structures, such as coupled via fields, breakouts, and plane gaps.

DDRX Design

- DDRx Wizard automates signal integrity and timing analysis; guides designers step by step through analysis of an entire DDR interface
- Supports multiple DDR, LPDDR and NV-DDR technologies, adapts data collection and simulation flows accordingly
- Optimizes On-Die Termination (ODT) settings using swept-parameter analysis to determine best settings
- Automatically computes design margins based on controller-specific write-leveling capabilities
- Models JEDEC DRAM parameters and controller capabilities
- Generates results with or without crosstalk
- Extensive results reporting provides design margin details, per-bit eye diagrams and measurement waveforms

SerDes Channel Design

- Compliance wizard includes built-in support for over 35 different standard protocols, including Ethernet, OIF-CEI, PCIe, Fiber Channel, USB, and JESD-based technologies
- Additional standards supported through design kits
- Built-in COM/JCOM analysis engine runs much faster than standard approaches and doesn't require additional third-party software licenses
- Full IBIS-AMI model support for vendor-specific flows
- Dedicated 3D EM solver creates parameterized single and differential models of vias and associated stitching vias
- Integrates with general-purpose 3D EM solver for modeling arbitrary structures and PCB sections

Supported PCB Layout Systems

- Tightly integrated with Mentor Graphics Xpedition™, PADS Professional® and PADS®
- Altium Designer (through ODB++)
- Cadence Allegro and OrCAD Layout tools
- Zuken CR Series

HyperLynx Product Family

HyperLynx SI is part of an integrated family of analysis tools for high-speed electronic design:

- Electrical design rule checking (DRC/ERC)
- Signal integrity analysis (SI)
- Power integrity analysis (PI)
- 3D electromagnetic modeling (3D EM)

For the latest product information, call us or visit: www.mentor.com/pcb

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